High-Resolution Low-Latency Capacitive Displacement Sensor

Sha Xia, Jeroen P. van Schieveen, Stoyan Nihtianov Nihtianov and Jo W. Spronck

Abstract - **This paper addresses the challenges related to the design of a high-resolution, low-latency capacitive displacement sensor. An auto-alignment mechanism of the sensor head is proposed which relaxes the resolution requirement of the readout circuit. Different interfacing principles are investigated and analyzed, and the advantage of using a switched-capacitor readout topology for a specific application is made clear.**

Keywords – **Capacitive position sensor, auto alignment, thermal slider**

I. INTRODUCTION

In many industrial applications, closed-loop control systems are needed to accurately position and align basically static objects. These objects can be critical parts of complex machines. An accurate displacement sensor is an indispensable element in such systems, because it measures the relative position and the drift/vibrations of the controlled objects. Such a sensor needs to provide high accuracy and high resolution with minimum latency imposed by the control system. In some applications, sub-nanometer accuracy needs to be achieved with a maximum stroke of the target of only a few micrometers. Although the dynamic range is within the scope of an absolute sensor, often laser interferometers or optical interferometric encoders are used because they can bridge the relatively high mounting tolerances of the complex machine, while still providing very high accuracy. Unfortunately, encoders and especially interferometers are bulky and very expensive. Their primary field of application is for position measurement of moving objects with large stroke. For applications where only a range of a few micrometers measurement needs to be covered, capacitive sensors offer a reliable low-power, low-noise alternative. They are relatively cheap, compact and robust, and therefore they are very attractive for sub-nanometer displacement measurements.

Unfortunately, correct alignment of the sensor head to a distance close to a few micrometers is in most cases not possible without any special measures. The resulting gap distance is too large for current electronics to achieve the desired resolution. The alignment problems can be eventually solved with a more accurate assembly of the machine, but the resulting increase in assembly costs, and hence the overall machine costs, would eliminate the cost advantage of using a capacitive sensor instead of using expensive optical linear encoders.

As opposed to targeted measurement ranges of only a few micrometers, a relatively large stand-off distance creates a great challenge for the readout circuit design. The presence of this stand-off distance considerably degrades the sensitivity of the sensor, as the sensitivity of the capacitive displacement sensor is inversely proportional to the square of the distance between its plates [1]. On the other hand, the resulting increased ratio between offset capacitance and sensing capacitance (capacitance variation) poses a very stringent dynamic range requirement for the readout circuit.

The effect of the offset capacitance can be cancelled electrically by connecting a fixed capacitance to form a capacitance half-bridge and driving the two ends of the half-bridge with an anti-phase excitation signal, as shown in Fig. 1. For convenience, we will hereafter refer to this approach as the "electrical zoom-in". In practice, when the zoom-in factor needs to be in the order of 50 to 100, the realization requires very careful matching of the excitation signal along with high initial accuracy and low drift for the fixed capacitance. Eventually the electrical zoom-in principle stops functioning correctly.

A far more attractive solution is to try to reduce the initial distance of the sensor plates to lower values without relying on expensive assembly or machining processes. An alignment system, which adds the functionality to the sensor head in order to move and align the plates of the capacitive sensor after mounting, would fulfill the above-mentioned task and greatly relax the specification of the readout circuitry. In [2] a simple, low-cost, compact and stable actuation mechanism has been proposed. Integrating this system inside a capacitive sensor-head could be a solution for mechanical zoom-in.

The design of a high-resolution, low-latency capacitive sensor system is clearly not only limited to pure electronics or mechanics. Therefore the design of this new capacitive sensor for industrial applications was created using a mechatronic design approach. The project was carried out in cooperation with both electrical and mechanical engineering. The combined concepts from both disciplines will be presented below.

This paper is organized in four sections. Section II describes the details of alignment problems and the mechanical zoom-in system. In section III detailed performance of electrical zoom-in and different readout

S. Xia is with Electronic Instrumentation Laboratory, Delft University of Technology - Netherlands, e-mail: s.xia@tudelft.nl
J. P. van Schieveen is with Departmet of Mechanical, Maritime and Materials Engineering, Delft University of Technology - Netherlands, e-mail: j.p.vanschieveen@tudelft.nl
S. Nihtianov is with Electronic Instrumentation Laboratory, Delft University of Technology - Netherlands, e-mail: s.nihtianov@tudelft.nl
J. W. Spronck is with Departmet of Mechanical, Maritime and Materials Engineering, Delft University of Technology - Netherlands, e-mail: j. w. spronck @tudelft.nl

topologies will be analyzed and assessed. The conclusion is given in section IV.

II. INTEGRATED ALIGNMENT SYSTEM

A. *Alignment error*

Like electrical zoom-in, electrode alignment or mechanical zoom-in has its own constraints. Practical limitations to the fabrication of the sensor head and especially the electrodes request for a minimal stand-off distance. A too small gap will result in unacceptable non-linearity of the sensor system.

The effect can be decreased by a larger nominal standoff, but this will increase the demands for the electronic read-out circuit. As the error increases rapidly with smaller distance, 10 um is a good trade of and will be used in further calculations.

B. *Alignment method*

Alignment of the sensor electrodes to an initial distance of 10 um with limited tilt after installation has been shown above to be an important part in the design of a high-resolution, high-speed capacitive sensors system. Therefore, a stable and cost-effective alignment method is necessary.

A new alignment mechanism has been presented in [2], the so-called 'thermal stepper'. The mechanism is compact, cost-effective and offers high stability. Thermal actuation is used to generate movements during the alignment procedure. As this is done by electrical heating, it can be operated only by applying the right electrical signals. This enables the use in confined spaces or non-accessible environment.

Fig. 1. shows a schematic drawing of the basic components of the system. The system consists of 12 clamping elements and a base that is machined out of one piece of metal. This guarantees stability and enables tight tolerances. The clamping elements use friction force to clasp an electrode and fix it in position.

Heaters on the clamping elements are used for thermal actuation. Applying heat in a defined sequence forces the electrode move relative to the base. In contrast to normal thermal actuation systems, the thermal stepper is able to create a permanent displacement, even after heat is no longer applied to the system.

One of the electrodes of a parallel plate system can be fixed using a non-adjustable sensor head. The second 'moving' electrode is positioned using the mechanism. The initial distance between the electrodes after installation is chosen to be large enough to overcome all machining and mounting tolerances. Prior to using the sensor system, the thermal stepper is activated. The moving electrode will move towards the fixed electrode. The stepping procedure ends when the electrode gap is small enough, i.e. when the measurement capacitance is larger than the offset cancellation capacitance. Final alignment is accomplished by heating all elements. Due to thermal expansion of the elements, the electrode displaces and eventually touches the fixed electrode. The allowed slip of the clamping system makes sure the electrodes end up parallel. Cooling down makes all of the elements contract and the moving electrode retracts over a fixed distance. This distance has a linear relation to the temperature step in the last heating phase. A well-defined temperature step ensures a well-defined electrode distance.

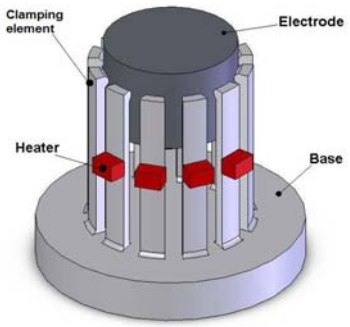

Fig. 1. Test setup of the thermal stepper alignment system. The actuator can be integrated in a sensor head to implement automatic alignment.

C. *Proposed system*

An integrated alignment system in the capacitive sensor head is assumed to be essential in combination with electrical zoom-in techniques. The combined system enables application of capacitive sensors in industrial applications without the need for high machining tolerances or costly assembly and alignment procedures.

Provisional specifications of the sensor head have been determined. These will be used as initial values for the design of the electronic read-out. Initial gap distance after adjustment will be 10 um with a tolerance of ± 0.1 um. Active electrode diameter will be 3.8mm, resulting in a nominal capacitance of 10pF. Tilt error calculations showed that maximum gap difference must be below 0.8 um.

III. CAPACITIVE SENSOR READOUT FRONT-ENDS

Auto-alignment principle alone cannot completely eliminate the offset capacitance. However, by merit of it, the electrical zoom-in can be applied with a reduced and more practical zoom-in factor to cancel the residual offset capacitance. The design challenge then falls on the front-end interface that converts capacitance variation into output voltage variation. The interface should also be able to tolerate large parasitic capacitance, since the sensor capacitance is off-chip and a guard-ring is needed to guarantee the linearity of the sensor. Capacitance readout can be based on capacitance-to-frequency, capacitance-to-charge, or capacitance-to-voltage conversion [4]. The first type requires a long conversion time to reach a high-resolution result and will therefore be not considered. Switched-capacitor (SC) front-end [5] and synchronous detection with a continuous-time (CT) front-end [6,7] are techniques commonly used to achieve high resolution

capacitance readout with reasonable speed. Both methods have their advantages and disadvantages.

A. Continuous-time readout circuits.

Continuous-time (CT) readout circuits make use of modulation and synchronous detection to readout the capacitive sensor and therefore they are very popular for high-resolution systems because of the low-noise performance inherent of continuous-time systems [6]. The front-end can be realized either with voltage-mode readout (voltage amplifier [6]) or with current-mode readout (charge amplifier [7]). Voltage-mode readout is very sensitive to parasitic capacitance and hence will be excluded in the following discussion.

The signal from the half-bridge can also be readout by a continuous-time current-mode (CTC) interface. Fig. 2 illustrates a charge amplifier interface. In this case, the central node of the bridge is held at virtual ground and the effect of the parasitic capacitance is thus reduced. The excitation signal is preferably sinusoidal to avoid errors induced by distortion. When the bandwidth of the charge amplifier is larger than the excitation frequency, the output voltage of the charge amplifier can be written as (assuming infinite loop-gain):

$$|V_{out}| = V_m \frac{\Delta C}{C_f} \tag{1}$$

The output noise of the charge amplifier can be calculated as:

$$\frac{\overline{v_{out}^2}}{\Delta f} = \overline{v_n^2} \cdot \left(\frac{C_T}{C_f}\right)^2 \tag{2}$$

where $C_T = C_s + C_r + C_p + C_f$ denotes the total capacitance at the virtual ground node, and v_n is the input referred noise voltage of the amplifier. Then the capacitance readout resolution for a given bandwidth (BW) is given by:

$$\Delta C_{min-rms} = \frac{C_T}{V_m} \cdot \overline{v_n} \cdot \sqrt{BW} \tag{3}$$

B. Switched-capacitor readout circuit

Switched-capacitor (SC) front-end is shown in Fig. 3. The resulting output voltage would then be a representation of the capacitance difference:

$$V_{out} = V_{exc} \frac{\Delta C}{C_f} \tag{4}$$

The reset switch will create a kT/(Cs+Cr+Cp) noise every time it opens. However, since this noise is effectively 'frozen' after the reset switch opens, the use of correlated double sampling (CDS) can effectively eliminates this noise, along with the effect of amplifier flicker noise and

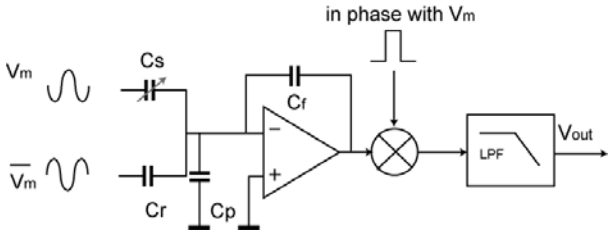

Fig. 2. Simplified block diagram of continuous-time capacitive readout circuits.

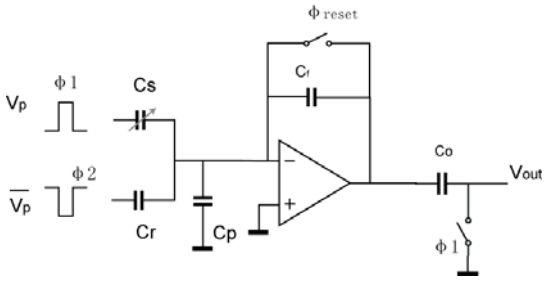

Fig. 3. Simplified diagram of switched-capacitor readout circuit.

offset. [5]. The wideband thermal noise of the amplifier is amplified and aliased into the base-band frequency range (DC to $\frac{f_s}{2}$) caused by the sampling process. The CDS process necessary to eliminate the flicker noise unfortunately simultaneously serves to double the white noise power. The total effective in-band noise power density can be calculated as [5]:

$$\frac{\overline{v_{out}^2}}{\Delta f} = \overline{v_n^2} \cdot \left(\frac{C_T}{C_f}\right)^2 \cdot \frac{\frac{\pi}{2} \cdot f_{-3db}}{\frac{f_s}{2}} \cdot 2 \tag{5}$$

where f_{-3db} denotes the cut-off frequency of the feedback amplifier and can be calculated as $f_{-3db} = F \cdot f_u$. F is the feedback factor, and f_u is the unity gain frequency of the amplifier. Therefore, the readout resolution for switched-capacitor readout circuit can be expressed as:

$$\Delta C_{min-rms} = \frac{C_T}{V_{exc}} \cdot \overline{v_n} \cdot \sqrt{BW} \cdot \sqrt{\frac{2\pi \cdot f_{-3db}}{f_s}} \tag{6}$$

C. Comparison

The last term in Eq. (6) is the noise penalty factor compared to the noise of continuous-time charge amplifier interface given in Eq. (3). equals where τ is the settling time constant. If half of the sampling period is available for settling, then the noise penalty factor works out to be $\sqrt{2 \cdot n_\tau}$, where n_τ is the number of settling time constants

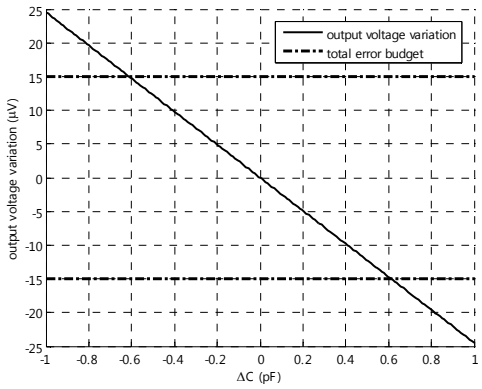

Fig. 4. Calculated variation in output voltage due to 1% parasitic capacitance change as a function of sensor capacitance when the amplifier gain at 1 MHz is assumed to be 200.

needed to reach the required dynamic settling error specification. In this case, n_T needs to be about 14 for a dynamic settling error less than 1ppm. Thus the noise power is 28 times higher in a switched-capacitor interface circuit then in a continuous-time charge amplifier interface.

In spite of the noise penalty, the SC interface has the advantage that the deviation from the ideal transfer function is essentially set by the DC gain of the amplifier because it sets the lower band for charge-transfer accuracy. By applying a gain-boosting technique, the DC gain of a single-stage amplifier can reach above 120dB.

The CT charge amplifier interface, however, suffers from the error introduced by insufficient loop gain at the excitation frequency, which needs to be at least a few hundred kilo hertz to satisfy latency requirements.

Complete analysis of fig. 2 taken into account of finite amplifier gain gives:

$$V_o = \frac{-V_m \cdot \Delta C}{\frac{\Delta C}{A} + \frac{C_p}{A} + \frac{1+A}{A} C_f} \qquad (7)$$

where C_p is the total input parasitic capacitance, C_f is the feedback capacitance, and A is the amplifier gain at excitation frequency.

Because the amplifier is used to drive a capacitive load, achieving a high gain at f_{exc} requires excessive power dissipation. For instance, if an amplifier gain of 200 is needed at 1 MHz while the effective load capacitance is 10 pF, the required g_m is 12.6 mS. In contrast, to satisfy noise performance, from (3) it can be calculated that $\overline{v_n}$ needs to be below 18.6 nV/√Hz to satisfy a capacitance resolution below 50 aF in 100 KHz bandwidth if C_T is 40 pF and V_m is 5V. If the noise of the input pair of the amplifier dominates, g_m only needs to be larger than 64 uS.

Also, an amplifier gain of 200 is not enough to tolerate variations in parasitic capacitance and gain values. Fig. 4 shows the calculated variation in output voltage due to 1% parasitic capacitance change as a function of the sensor capacitance change when the amplifier gain at 1 MHz is 200. The bold dotted line marks the limit for the tolerable drift from the system specification. It clearly shows that minor variation in the poorly-controlled parasitic capacitance value would cause the system to drift out of spec. On the other hand, SC readout circuit is highly insensitive to parasitic capacitance variation as long as sufficient DC gain is guaranteed.

Since the effective load capacitance is to some extent related to the value of the sensor capacitance, for small value capacitive sensors the requirement on g_m can be relaxed. Also if the sensor is integrated in the same chip as the readout circuit, the value of the parasitic capacitance can be greatly reduced. In these situations, the disadvantages of the CT readout circuit are less prominent therefore the CT readout circuit is favored for its superior noise performance. In the case where the nominal value of the capacitive sensor is in the order of 10 pF, and large parasitic capacitance exists, the SC readout circuit becomes more suitable.

IV. Conclusion

The design of a high-resolution, low-latency capacitive sensor system requires both mechanical design and electrical design efforts. A simple, cheap, compact and stable actuation principle has been proposed to realize auto-alignment of the sensor plates after mounting, which greatly reduces the dynamic range requirement for the readout circuit. Different types of capacitive readout circuits have been analyzed. For applications where sensor capacitance is in the order of 10 pF and parasitic capacitance is relatively large, switched-capacitor readout circuits show a clear advantage over continuous-time readout circuits with respect to stability. To make the best choice of interfacing topology of a capacitive sensor, the specific working conditions also need to be taken into account.

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